Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
11	244	717/146.ccls.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/05/25 08:06
L2	7	717/146.ccls. and (interface adj definition)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/05/25 08:27
L3	204	717/146.ccls. and ("data structure" or table or database or data-base or "data base")	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/05/25 08:09
L4	1	717/146.ccls. and ("hardware definition" or hdl)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/05/25 08:19
L5	7	I2 and I3	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ÖN	2005/05/25 08:22
L6	161	717/110.ccls.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/05/25 08:22
L7	111	717/110.ccls. and ("interface definition" or datastructure or "data structure" or tabel or database or data-base or "data base" or hdl or "hardware definition")	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/05/25 08:24
L8	0	717/110.ccls. and ("interface definition" or datastructure or "data structure" or tabel or database or data-base or "data base") and (hdl or "hardware definition")	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/05/25 08:24
L9	0	717/109.ccls. and ("interface definition" or datastructure or "data structure" or tabel or database or data-base or "data base") and (hdl or "hardware definition")	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/05/25 08:26

L10	272	717/109.ccls.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/05/25 08:25
L11	343	717/136.ccls.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/05/25 08:25
L12	5	717/136.ccls. and ("interface definition" or datastructure or "data structure" or tabel or database or data-base or "data base") and (hdl or "hardware definition")	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/05/25 08:26
S1	451	(HDL or (hardware adj description)) same (intermediate or IL) and (table or (data adj structure) or data-structure or (row near5 column))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/05/25 08:05
S2	90	(HDL or (hardware adj description)) same (intermediate or IL) same (translat\$4 or transform\$5 or compil\$5) and (table or (data adj structure) or data-structure or (row near5 column))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/08/25 16:10
S3	40209	object and interface and signal and port and input and output	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/08/25 16:12
S4	79	((HDL or (hardware adj description)) same (intermediate or IL) and (table or (data adj structure) or data-structure or (row near5 column))) and (object and interface and signal and port and input and output)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/08/25 16:13
S5	44	((HDL or (hardware adj description)) same (intermediate or IL) same (translat\$4 or transform\$5 or compil\$5) and (table or (data adj structure) or data-structure or (row near5 column))) and (object and interface and signal and port and input and output)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/08/25 17:06

S6	9	("5754826" "5870588" "5872810" "5987239" "6053947" "6152612" "6173435" "6421634" "6421818").PN.	USPAT	OR	OFF	2004/08/25 16:22
S7	2759	database and ((hardware adj description) or (interface adj definition) or hdl)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/08/25 17:08
S8	404	(database and ((hardware adj description) or (interface adj definition) or hdl)) and (object and interface and signal and port and input and output)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/08/25 17:08
S9	506	database same ((hardware adj description) or (interface adj definition) or hdl)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/08/25 17:08
S10	94	(database same ((hardware adj description) or (interface adj definition) or hdl)) and (object and interface and signal and port and input and output)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/08/25 17:09
S11	1	(database same ((hardware adj description) or (interface adj definition) or hdl)) and (object and interface and signal and port and input and output) and ((HDL or (hardware adj description)) same (intermediate or IL) same (translat\$4 or transform\$5 or compil\$5) and (table or (data adj structure) or data-structure or (row near5 column)))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/08/25 17:09
S12	10	"6132109".URPN.	USPAT	OR	OFF	2004/08/25 17:11
S13	6	"6132109".URPN. and (database or row or column)	USPAT	OR	OFF	2004/08/25 17:12

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S14	43	("5128871" "5220512"	USPAT	OR	OFF	2004/08/25 17:14
		"5258919" "5506788"			1	
		"5513119" "5553002"				
		"5629857" "5666289"				
		"5828581" "5852564"				
		"5889677" "5892678"				
	,	"5933356" "5963724"				
		"6044211" "6053947"				
		"6066179" "6106568"		1		
		"6117183" "6120549"		ļ		·
		"6132109" "6135647"				
		"6152612" "6205573"				
		"6219822" "6233723"				
1		"6236956" "6260179"				
		"6272671" "6298468"				
		"6311309" "6324678"				
		"6366874" "6378115"				
1		"6401230" "6449762"				
		"6457164" "6477683"			1	
		"6477689" "6480985"				
1		"6487698" "6505341"			,	
	1	"6519755" "2001/0018758"				
		"2002/0023256" I				
		"2002/0042904"				'
		"2002/0046386"				
		"2002/00 4 9957"	1			
		"2002/0166100"				
		"2003/0005396"				
1		"2003/0016206"				,
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S15	30	(("5128871" "5220512" "5258919" "5506788" "5513119" "5553002" "5629857" "5666289" "5828581" "5852564" "5889677" "5892678" "5933356" "5963724" "6044211" "6053947" "6066179" "6106568" "6117183" "6120549" "6132109" "6135647" "6152612" "6205573" "6219822" "6233723" "6236956" "6260179" "6272671" "6298468" "6311309" "6324678" "6366874" "6378115" "6401230" "6449762" "6457164" "6477683" "6477689" "6480985" "6487698" "6505341" "6519755" "2001/0018758" "2002/0042904" "2002/0042904" "2002/0049957" "2002/0166100" "2003/0016246").PN.) and (database or row or column)	USPAT	OR	ON	2004/08/25 17:41
S16	160	717/136.ccls.	USPAT	OR	ON	2004/08/25 17:42
S17	188	717/146.ccls.	USPAT	OR	ON	2004/08/25 17:42
S18	1	(interface adj definition) same (compil\$5 or translat\$3) same intermediate same (table or database or data-base)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/08/30 08:52
S19	1	"5943674".URPN.	USPAT	OR	OFF	2004/08/30 08:47
S20	11	("5493675" "5577253" "5613117" "5640567" "5659753" "5671416" "5675805" "5701490" "5758163" "5761511" "5768564").PN.	USPAT	OR	OFF	2004/08/30 08:50
S21	0	(interface adj definition) same (front-end or (front adj end)) same intermediate same (table or database or data-base)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/08/30 08:53

S22	0	((interface adj definition)or idl)same (front-end or (front adj end)) same intermediate same (table or database or data-base)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/08/30 08:53
S23	0	((interface adj definition)or idl)same (front-end or (front adj end)) same intermediate same (table or database or data-base)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2004/08/30:08:55
S24	0	(hdl)same (front-end or (front adj end)) same intermediate same (table or database or data-base)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2004/08/30 08:54
S25	0	(hdl)same (front-end or (front adj end)) same intermediate	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2004/08/30 08:54
S26	16	(hdl)same (front-end or (front adj end)) same (table or database or data-base)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2004/08/30 08:55
S27	9	((interface adj definition)or idl)same (front-end or (front adj end)) same (table or database or data-base)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2004/08/30 08:55
S28	25	((hdl)same (front-end or (front adj end)) same (table or database or data-base)) or (((interface adj definition)or idl)same (front-end or (front adj end)) same (table or database or data-base))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2004/08/30 09:07
S29	25	(((hdl)same (front-end or (front adj end)) same (table or database or data-base)) or (((interface adj definition)or idl)same (front-end or (front adj end)) same (table or database or data-base))) and object	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2004/08/30 09:07
S30	0	activeupdate	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/09/02 18:56

S31	2	(object adj table) and (interface adj table) and ((link near3 object) near3 table)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/05/17 13:44
S32	2621	interface adj definition	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/05/17 14:10
S33	2	(interface adj definition) near5 (intermediate adj format)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/05/17 13:46
S34	89	(interface adj definition) near5 (table or database or row or column)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/05/17 13:48
S35	50	(interface adj definition) near5 (table or database or row or column) and (link\$3) and object and interface	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/05/17 13:49
S36	8	("5495567" "5550971" "5920725" "5970490" "6012067" "6289382" "6349302" "6430556").PN.	US-PGPUB; USPAT; USOCR	OR	OFF	2005/05/17 14:04
S37	44	(convert\$3 or transform\$3) near3 (interface adj definition)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/05/17 14:14
S38	43	S37 not S35	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/05/17 14:49
S39	639	(hdl or (descriptive and language)) near5 (database or data-base or (data adj base) or table)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/05/17 14:51
S40	Ō	(hdl or (descriptive and language)) near5 (database or data-base or (data adj base) or table) same (interface adj definition)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/05/17 14:54

S41	41	(hdl or (descriptive and language)) near5 (database or data-base or (data adj base) or table) same (interface)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/05/17 14:54
S42	41	(hdl or (descriptive and language)) near5 (database or data-base or (data adj base) or table) same (interface) and (object link interface row column source intermediate)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/05/17 15:00
S43	29	(hdl or (descriptive adj language)) near5 (database or data-base or (data adj base) or table) same (interface) and (object link interface row column source intermediate)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/05/17 15:15
S44	40	707/???.ccis. and hdl	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/05/17 15:21
S45	6760	707/10?.ccls.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/05/17 15:21
S46	122	707/10?.ccls. and "interface definitions"	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/05/17 15:22
S47	122	707/10?.ccls. and "interface definitions" and (object link interface row column source intermediate)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/05/17 15:40
S48	60	707/102.ccls. and "interface definitions" and (object link interface row column source intermediate)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/05/17 15:40
S49	2946	707/102.ccls.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/05/17 15:40
S50	60	707/102.ccls. and "interface definitions"	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/05/17 16:01

S51	20	olap and "interface definition"	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/05/17 15:44
S52	9	olap and (hdl or "description language")	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/05/17 15:46
S53	41	717/108.ccls. and "interface definitions"	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/05/17 16:01
S54	7	717/146.ccls. and "interface definitions"	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/05/17 16:02
S55	344	717/108.ccls.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/05/17 16:02



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1 Generation of the HDL-A-Model of a Micromembrane from Its Finite-Element-Description Klaus Hofmann, Manfred Glesner, Nicu Sebe, A. Manolescu, Santiago Marco, Josep Samitier, Jean-Michel Karam, Bernard Courtois

March 1997 Proceedings of the 1997 European conference on Design and Test

Full text available: pdf(574.37

KB) (1)

Additional Information: full citation, abstract

Publisher Site

A CAD tool for the automated generation of behavioral models in HDL-A is presented. This CAD tool has been implemented in the frame of a project for the automatic modeling of microsystem components for the co-simulation with VHDL or Spice-models. Starting from the finite-element-description of a microcomponent a nonlinear behavioral HDL-A-model is generated by successively adding or deleting effects to the HDL-A-model according to the observed differences between the two models. Using the exampl ...

Keywords: logic CAD, HDL-A-model, micromembrane, finite-element-description, CAD tool, automated generation, behavioral models, FEM, microsystem components, automatic modeling, cosimulation, VHDL-models, Spice-models

2 Probabilistic Models of Database Locking: Solutions, Computational Algorithms, and Asymptotics Debasis Mitra, P. J. Weinberger

September 1984 Journal of the ACM (JACM), Volume 31 Issue 4

Full text available: pdf(1.01 MB)

Additional Information: <u>full citation</u>, <u>references</u>, <u>citings</u>, <u>index</u> <u>terms</u>, <u>review</u>

3 On compiling queries in recursive first-order databases

Lawrence J. Henschen, Shamim A. Naqvi

January 1984 Journal of the ACM (JACM), Volume 31 Issue 1

Full text available: pdf(1.85 MB)

Additional Information: full citation, references, citings, index

terms, review

4 Useless Actions Make a Difference: Strict Serializability of Database Updates

Ravi Sethi

April 1982 Journal of the ACM (JACM), Volume 29 Issue 2

Full text available: pdf(502.75 Additional Information: full citation, references, citings, index terms

5 Preserving HDL synthesis hierarchy for cell placement

Yu-Wen Tsay, Wen-Jong Fang, Allen C.-H. Wu, Youn-Long Lin

April 1997 Proceedings of the 1997 international symposium on Physical design

Full text available: pdf(703.43 Additional Information: full citation, references, citings, index terms

6 Database theory—past and future

J. D. Ullman

June 1987 Proceedings of the sixth ACM SIGACT-SIGMOD-SIGART symposium on Principles of database systems

Full text available: pdf(1.07 Additional Information: full citation, abstract, references, citings, index terms

We briefly sketch the development of the various branches of database theory. One important branch is the theory of relational databases, including such areas as dependency theory, universal-relation theory, and hypergraph theory. A second important branch is the theory of concurrency control and distributed databases. Two other branches have not in the past been given the attention they deserve. One of these is "logic and databases," and the second is "object-oriented dat ...

7 A generalized model for a relational temporal database

Shashi K. Gadia, Chuen-Sing Yeung

June 1988 ACM SIGMOD Record, Proceedings of the 1988 ACM SIGMOD international conference on Management of data, Volume 17 Issue 3

Full text available: pdf(1.04 Additional Information: full citation, abstract, references, citings, index terms

We propose a generalized relational model for a temporal database which allows time stamping with respect to a Boolean algebra of multidimensional time stamps. The interplay between the various temporal dimensions is symmetric. As an application, a two dimensional model which allows objects with real world and transaction oriented time stamps is discussed. The two dimensional model can be used to query the past states of the database. It can also be used to give a precise classification of ...

8 Overview of the Jasmin database machine

Daniel H Fishman, Ming-Yee Lai, W Kevin Wilkinson

June 1984 ACM SIGMOD Record, Proceedings of the 1984 ACM SIGMOD international conference on Management of data, Volume 14 Issue 2

Full text available: pdf(648.31 KB) Additional Information: full citation, abstract, references, citings

The Jasmin database machine is being implemented as part of a research project in distributed processing and database management A primary goal of the work is to demonstrate the feasibility of a practical multiprocessor database machine suitable for large database, high transaction-rate applications Key features of Jasmin are its configurable performance, its use of off-the-shelf parts, and its ability to handle distributed databases A uniprocessor prototype of Jasmin has already been completed ...

9 <u>Simplifying distributed database systems design by using a broadcast network</u> Jo-Mei Chang

June 1984 ACM SIGMOD Record, Proceedings of the 1984 ACM SIGMOD international conference on Management of data, Volume 14 Issue 2

Full text available: pdf(1.36 MB)

Additional Information: full citation, abstract, references, citings

Atomic broadcast and failure detection are powerful primitives for distributed database systems In the distributed database system LAMBDA, they are provided as network primitives In this paper, we show how atomic broadcast and failure detection simplify transaction commitment, concurrency control, and crash recovery Specifically, we give a simple two-phase non-blocking commit protocol, whereas three phases are required in a point-to-point network We also give a simplified read-one/write-a ...

10 Precedent-based manipulation of VLSI structures

Richard H. Lathrop, Robert S. Kirk

July 1986 Proceedings of the 23rd ACM/IEEE conference on Design automation

Full text available: pdf(522.17 Additional Information: full citation, abstract, references, index terms

CONSTELLATION, a general LISP-based tool for structure recognition and manipulation, is described. CONSTELLATION is a design refinement tool for the later stages of the design process, when a complete (or nearly so) design is available. It is intended to recognize local substructures in the design and carry out specific associated manipulations. The recognition phase is driven by a design precedent. This is a pattern which an experienced designer points out in an existing ...

11 A graphical data management system for HDL-based ASIC design projects

C. Mayer, J. Pleickhardt, H. Sahm

September 1996 Proceedings of the conference on European design automation

Full text available: pdf(311.58 Additional Information: full citation, references, citings, index terms

12 EASE: a design support environment for the HDDL ELLA

J. D. Morison, N. E. Peeling, T. L. Thorp, E. iV. Whiting

October 1987 Proceedings of the 24th ACM/IEEE conference on Design automation

Full text available: pdf(940.53 Additional Information: full citation, abstract, references, index terms

This paper describes the ELLA applications support environment - EASE. The support environment allows separate modular compilation and multi-level simulation with almost no semantic or syntatic constructs in the ELLA language. The paper describes the form that the

EASE takes and the advantages this gives over other programming support environments. The weaknesses of the current EASE and future work are also discussed.

13 Linking codesign and reuse in embedded systems design

M. Meerwein, C. Baumgartner, W. Glauert

May 2000 Proceedings of the eighth international workshop on Hardware/software codesign

Full text available: pdf(77.16 Additional Information: full citation, abstract, references, citings, index terms

This paper presents a complete codesign environment for embedded systems which combines automatic partitioning with reuse from a module database. Special emphasis has been put on satisfying the requirements of industrial design practice and on the technical and economic constraints associated with automotive control applications. The object-oriented database architecture allows efficient management of a large number of modules. Experimental results from a real-world example demonstr ...

14 Towards design and validation of mixed-technology SOCs

S. Mir, B. Charlot, G. Nicolescu, P. Coste, F. Parrain, N. Zergainoh, B. Courtois, A. Jerraya, M. Rencz

March 2000 Proceedings of the 10th Great Lakes symposium on VLSI

Full text available: pdf(581.54 Additional Information: full citation, abstract, references, index terms

This paper illustrates an approach to design and validation of heterogeneous systems. The emphasis is placed on devices which incorporate MEMS parts in either a single mixed-technology (CMOS + micromachining) SOC device, or alternatively as a hybrid system with the MEMS part in a separate chip. The design flow is general, and it is illustrated for the case of applications embedding CMOS sensors. In particular, applications based on finger-print recognition are considered since a ric ...

Keywords: HDLs, MEMS, SOCs, architecture exploration, cosimulation, design, verification

15 On the Desirability of Acyclic Database Schemes

Catriel Beeri, Ronald Fagin, David Maier, Mihalis Yannakakis

July 1983 Journal of the ACM (JACM), Volume 30 Issue 3

Full text available: pdf(2.10 Additional Information: full citation, references, citings, index terms

16 A timing-driven soft-macro resynthesis method in interaction with chip floorplanning

Hsiao-Pin Su, Allen C.-H. Wu, Youn-Long Lin

June 1999 Proceedings of the 36th ACM/IEEE conference on Design automation

Full text available: pdf(371.78 Additional Information: full citation, references, citings, index terms

17
<u>Testbench, verification and debugging: practical considerations: Advanced techniques for RTL debugging</u>

Yu-Chin Hsu, Bassam Tabbara, Yirng-An Chen, Furshing Tsai

June 2003 Proceedings of the 40th conference on Design automation

Full text available: pdf(359.48 Additional Information: full citation, abstract, references, index terms

Conventional register transfer level (RTL) debugging is based on overlaying simulation results on structural connectivity information of the Hardware Description Language (HDL) source. This process is helpful in locating errors but does little to help designers reason about the how and why Designers usually have to build a mental image of how data is propagated and used over the simulation run. As designs get more and more complex, there is a need to facilitate this reasoning process, and autom ...

Keywords: debug, reasoning, simulation, verification, visualization

18 HDM—a model-based approach to hypertext application design

Franca Garzotto, Paolo Paolini, Daniel Schwabe

January 1993 ACM Transactions on Information Systems (TOIS), Volume 11 Issue 1

Full text available: pdf(1.94 Additional Information: full citation, abstract, references, citings, index terms, review

Hypertext development should benefit from a systematic, structured development, especially in the case of large and complex applications. A structured approach to hypertext development suggests the notion of authoring-in-the-large. Authoring-in-the-large allows the description of overall classes of information elements and navigational structures of complex applications without much concern with implementation details, and in a system-independent manner. The paper presents ...

Keywords: HDM, derived links, hypertext applications, hypertext design models, hypertext structures

19 A heuristic chip-level test generation algorithm

Daniel S. Barclay, James R. Armstrong

July 1986 Proceedings of the 23rd ACM/IEEE conference on Design automation

Full text available: pdf(556.00 Additional Information: full citation, abstract, references, citings, index terms

An algorithm is given for generating tests from chip-level functional descriptions. The algorithm uses a chip-level fault model to define faults and fault sensitization requirements, and uses the hardware description language (HDL) definition to solve for the test vector. Artificial intelligence techniques of goal trees and rule databases are use to implement the algorithm in ProLog. The goal types and solving strategies are outlined. The current, partial ProLog implementation is discussed. ...

20 Session 6B: Convergence of abstractions in high-level synthesis: A system for synthesizing optimized FPGA hardware from MATLAB

Malay Haldar, Anshuman Nayak, Alok Choudhary, Prith Banerjee

November 2001 Proceedings of the 2001 IEEE/ACM international conference on Computer-aided design

Full text available: pdf(158.74 Additional Information: full citation, abstract, references, citings,

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index terms

Efficient high level design tools that can map behavioral descriptions to FPGA architectures are one of the key requirements to fully leverage FPGA for high throughput computations and meet time-to-market pressures. We present a compiler that takes as input algorithms described in MATLAB and generates RTL VHDL. The RTL VHDL then can be mapped to FPGAs using existing commercial tools. The input application is mapped to multiple FPGAs by parallelizing the application and embedding communication an ...

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1 Preserving HDL synthesis hierarchy for cell placement

Yu-Wen Tsay, Wen-Jong Fang, Allen C.-H. Wu, Youn-Long Lin

April 1997 Proceedings of the 1997 international symposium on Physical design

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Full text available: pdf(703.43 Additional Information: full citation, references, citings, index terms

2 A timing-driven soft-macro resynthesis method in interaction with chip floorplanning Hsiao-Pin Su, Allen C.-H. Wu, Youn-Long Lin

June 1999 Proceedings of the 36th ACM/IEEE conference on Design automation

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Full text available: pdf(371.78 Additional Information: full citation, references, citings, index terms

3 Linking codesign and reuse in embedded systems design

M. Meerwein, C. Baumgartner, W. Glauert

May 2000 Proceedings of the eighth international workshop on Hardware/software codesign

Full text available: pdf(77.16 KB)

Additional Information: full citation, abstract, references, citings, index terms

This paper presents a complete codesign environment for embedded systems which combines automatic partitioning with reuse from a module database. Special emphasis has been put on satisfying the requirements of industrial design practice and on the technical and economic constraints associated with automotive control applications. The object-oriented database architecture allows efficient management of a large number of modules. Experimental results from a real-world example demonstr ...



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EEEE	IEEE		Custom Integrated Circuits Conference, 1993., Proceedings of the 9-12 May 1993 Page(s):13.2.1 - 13.2.4
CNF	Conference		AbstractPlus Full Text: PDF(340 KB) IEEE CNF
CNF	Proceeding IEE Conference Proceeding		2. Synthesis of customised hardware from ADA Dossis, M.F.; Noras, J.M.; Porter, G.J.; Circuits and Systems, 1994. ISCAS '94., 1994 IEEE International on Volume 1, 30 May-2 June 1994 Page(s):229 - 232 vol.1
IEEE STD	IEEE Standard		AbstractPlus Full Text: PDF(288 KB) IEEE CNF
<u>.</u> .			3. HDL optimization using timed decision tables Jian Li; Gupta, R.K.; Design Automation Conference Proceedings 1996, 33rd 3-7 June 1996 Page(s):51 - 54
			AbstractPlus Full Text: PDF(364 KB) IEEE CNF
			4. A multidatabase system implementation on CORBA Dogac, A.; Dengi, C.; Kilic, E.; Ozhan, G.; Ozcan, F.; Nural, S.; E C.; Halici, U.; Arpinar, B.; Koksal, P.; Mancuhan, S.; Research Issues in Data Engineering, 1996. Interoperability of No. Database Systems. Proceedings. Sixth International Workshop on 26-27 Feb. 1996 Page(s):2 - 11
			AbstractPlus Full Text: PDF(952 KB) IEEE CNF
			5. Design of a DBMS for VHDL-based CAD environments Venkatesan, S.; Davis, K.C.; Design Automation Conference, 1995. Proceedings of the ASP-D, '95/CHDL '95/VLSI '95., IFIP International Conference on Hardw Description Languages; IFIP International Conference on Very La Integration., Asian and South Pacific

29 Aug.-1 Sept. 1995 Page(s):539 - 544 AbstractPlus | Full Text: PDF(620 KB) IEEE CNF 6. HDL code restructuring using timed decision tables Jian Li; Gupta, R.K.; Hardware/Software Codesign, 1998. (CODES/CASHE '98) Proced Sixth International Workshop on 15-18 March 1998 Page(s):131 - 135 AbstractPlus | Full Text: PDF(200 KB) IEEE CNF 7. COMPCON Spring '90: Thirty-Fifth IEEE Computer Society International Conference. Intellectual Leverage. Digest of Pap No.90CH2843-1) Compcon Spring '90. 'Intellectual Leverage'. Digest of Papers. Thi IEEE Computer Society International Conference. 26 Feb.-2 March 1990 AbstractPlus | Full Text: PDF(36 KB) THEE CNF 8. MediaWare: a distributed multimedia environment with inter Al-Salqan, Y.Y.; Chang, C.K.; Enabling Technologies: Infrastructure for Collaborative Enterprise ___ Proceedings of the Fourth Workshop on 20-22 April 1995 Page(s):128 - 137 AbstractPlus | Full Text: PDF(560 KB) IEEE CNF 9. Decomposition of timed decision tables and its use in presynth-optimizations Jian Li; Gupta, R.K.; Computer-Aided Design, 1997. Digest of Technical Papers., 1997 International Conference on 9-13 Nov. 1997 Page(s):22 - 27 AbstractPlus | Full Text: PDF(496 KB) | IEEE CNF 10. HDL presynthesis optimizations using a tabular model Jian Li; Gupta, R.K.: Very Large Scale Integration (VLSI) Systems, IEEE Transactions Volume 8, Issue 4, Aug. 2000 Page(s):369 - 378 AbstractPlus | References | Full Text: PDF(164 KB) | IEEE JNL 11. Generating the optimal graph representations from the instru tables of circuits Chen, C.Y.R.; Tseng, W.-C.; Custom Integrated Circuits Conference, 1994., Proceedings of the 1-4 May 1994 Page(s):241 - 244 AbstractPlus | Full Text: PDF(384 KB) IEEE CNF 12. Hardware/software cosynthesis: multiple constraint satisfaction component retrieval Miller, R.; Carter, H.; Davis, K.; Venkatesan, S. Engineering of Complex Computer Systems, 1996. Proceedings. International Conference on 21-25 Oct. 1996 Page(s):383 - 390 AbstractPlus | Full Text: PDF(856 KB) IEEE CNF 13. Accurate high level datapath power estimation Crenshaw, J.E.; Sarrafzadeh, M.; European Design and Test Conférence, 1997. ED&TC 97. Procee 17-20 March 1997 Page(s):590 - 596

AbstractPlus | Full Text: PDF(580 KB) IEEE CNF 14. Diagonal examples for design space exploration in an education environment City-1
Takahashi, R.; Yoshida, N.;
Microelectronic Systems Education, 1999. MSE '99. IEEE Internations Conference on 19-21 July 1999 Page(s):71 - 73 AbstractPlus | Full Text: PDF(88 KB) IEEE CNF 15. Layout synthesis of combinational blocks from behavioral har descriptions Wu, Q.; Ramirez-Chavez, S.R.; ASIC Conference and Exhibit, 1992., Proceedings of Fifth Annua International 21-25 Sept. 1992 Page(s):38 - 41 AbstractPlus | Full Text: PDF(276 KB) IEEE CNF 16. A very large scale integrated circuits design laboratory for undergraduates Erickson, G., Daniels, P., Clark, R., Frontiers in Education Conference, 1993. Twenty-Third Annual C 'Engineering Education: Renewing America's Technology', Proce-6-9 Nov. 1993 Page(s):419 - 421 AbstractPlus | Full Text: PDF(216 KB) | IEEE CNF 17. Distributed VHDL simulation within a workstation cluster ___ Koch, M.; Tavangarian, D. System Sciences, 1994. Vol.II: Software Technology, Proceeding Twenty-Seventh Hawaii International Conference on Volume 2, 4-7 Jan. 1994 Page(s):313 - 322 AbstractPlus | Full Text: PDF(696 KB) | IEEE CNF 18. Verilog netlist as an exchange language Jen-Jen Lung; Bhasker, J.; Verilog HDL Conference, 1994., International 14-16 March 1994 Page(s):10 - 14 AbstractPlus | Full Text: PDF(220 KB) IEEE CNF 19. Performance and area estimation based on VHDL description functional unit database Tao Wang; Haggard, R.L.; System Theory, 1995., Proceedings of the Twenty-Seventh South Symposium on 12-14 March 1995 Page(s):379 - 383 AbstractPlus | Full Text: PDF(340 KB) | IEEE CNF 20. A radix-2 general division algorithm with carry-free scheme a divider implementation
Jen-Shiun Chiang; Hung-Da Chung; Ming-Hsou Tsai;
Electronics, Circuits and Systems, 1999. Proceedings of ICECS 'S IEEE International Conference on Volume 1, 5-8 Sept. 1999 Page(s):569 - 572 vol.1 AbstractPlus | Full Text: PDF(260 KB) | IEEE CNF

21. Knowledge based automatic simulation model generation syst

Circuits, Devices and Systems, IEE Proceedings [see also IEE Pro

Kang, S.

Circuits, Devices and Systems]
Volume 144, Issue 2, April 1997 Page(s):88 - 96
AbstractPlus | Full Text: PDF(876 KB) IEE INL

22. A mixed level simulator mega-FAL with novel data structure HDL statements

Ainara, M.; Sekine, M.; Custom Integrated Circuits Conference, 1990., Proceedings of the 13-16 May 1990 Page(s):10.3/1 - 10.3/4 AbstractPlus | Full Text: PDF(320 KB)

23. Industrial experimentation of high-level synthesis
Kission, P.; Closse, E.; Bergher, L.; Jerraya, A.A.;
Design Automation Conference, 1993, with EURO-VHDL '93. P1
EURO-DAC '93. European
20-24 Sept. 1993 Page(s):506 - 511
AbstractPlus | Full Text: PDF(456 KB) IEEE CNF

24. An electro-optical standard-cell for ASIC design
Seyfou, S.; Auletta, R.;
ASIC Conference and Exhibit, 1994. Proceedings., Seventh Annu
International
19-23 Sept. 1994 Page(s):22 - 24
AbstractPlus | Full Text: PDF(236 KB) IEEE CNF

25. An FPGA-based point pattern matching processor with applic fingerprint matching
Ratha, N.K.; Jain, A.K.; Rover, D.T.;
Computer Architectures for Machine Perception, 1995. Proceedin '95
18-20 Sept. 1995 Page(s):394 - 401
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